REMARKS/ARGUMENTS

The Examiner's final Restriction Request is acknowledged and non-elected claims 7-11, 19-22 and 24-32 have been canceled. A divisional application will be filed at a later date.

Examiner Paul E. Brock II is thanked for thoroughly reviewing the subject application. Examiner is also thanked for the indication of allowing claims 6 and 18 if these claims are rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1-6, 12-18 and 23 are pending under this Office Action.

All claims are believed to be in condition for allowance.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claims 1-5 and 12-17 under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent 6,143,579) in view of Yang (U.S. Patent 5,913,102) and Ahn (U.S. Patent 5,563,080) is respectfully requested based on the following.

Chang et al. provides for monitoring gate oxide damage by monitoring the status of a plasma etching tool with regard to the tendency of the tool to introduce plasma damage in thin gate and tunnel layers.

For this purpose Chang et al. provides for the following steps, highlighted in summary form:

- a plurality of monitoring wafers are created (see text provided by Chang et al. col. 3, lines 45 e.a.), each monitoring wafer, as shown in the cross section of Fig. 1 of Chang et al., comprises regions 12 of FOX, gate oxide 14 interposed between the FOX regions 12 and a blanket layer of poly deposited over the substrate 10.
- at the time that a plasma etch tool is to be evaluated, one of the monitoring wafers is selected for that purpose, the poly 16 is patterned, partially exposing the gate oxide 14, an edge of the patterned polysilicon is located across the thin film gate oxide 14, then a layer 22 of sidewall insulation material, such as silicon oxide, is deposited after which the monitoring wafer, shown in cross section in Fig. 2C, is placed into the etching tool that is to be evaluated

- the etching tool under evaluation is used to etch the layer 22 of sidewall insulation material, specifically to form a sidewall over the edge of the patterned polysilicon since such a process, see text col. 4, lines 2 e.a., is particularly prone to cause gate or tunnel oxide degradation since, at that time, the patterned layer of poly (the isolated conductive layer) is for the first time exposed to the plasma that is used to create the sidewall
- the above highlighted processing steps are performed using the monitoring wafer, that is the steps of sidewall etching, see text col. 4, lines 13 e.a., prior to executing a test recipe. That is to say, using a monitoring wafer which comprises a patterned layer of poly, patterned such that an edge of the patterned layer of poly overlies a thin layer of gate oxide, so that a sidewall can be created there-over, first exposing the poly and exposing the gate oxide, over which a layer of sidewall insulation material has been deposited, the sidewall is created by executing the test recipe on the monitoring wafer that has been placed in a tool in which the test recipe will be executed, exposing the gate oxide, after which the exposed gate oxide of the monitoring wafer is evaluated for damage by performing Q_{BD} and E_{BD}

measurements on the gate oxide. This latter sequence is one instance of evaluation, a plurality of such instances is used to accumulate a history of gate oxide damage for a particular tool and for particular etch procedures.

Conclusions that can be drawn from the above summary of the Chang invention are the following:

- the Chang invention provides a destructive test whereby a monitoring wafer is etched in order to evaluate a new etch recipe; the claimed invention provides a method whereby a monitoring wafer can be used without permanently affecting or damaging the monitoring wafer
- the monitor wafer of the claimed invention, after the procedure of the invention of monitoring a processing environment has been completed, can be restored to its original condition by applying an anneal to the monitor wafer. This anneal releases the trapped electron charge. The monitor wafer can after this be re-used
- the method of the claimed invention monitors electron charging during the creation of a semiconductor device

- the method of the invention makes use of electron trapping that occurs as a result of FN tunneling in a layer of interlayer oxide of an EPROM device
- the electron trapping is monitored under conditions of processing. After the electron trapping has occurred, the rate of charge trapped in interlayer oxide is measured during Wafer Acceptance Testing (WAT)
- the structure that is provided by Chang et al. is significantly different from the structure that is provided by the claimed invention, as is clear when Figs. 2C and 4 provided by Chang et al. are compared with Fig. 10 of the claimed invention, and
- the parameters that are used by Chang et al. to monitor gate oxide damage, that is charge-to-breakdown and the breakdown field, are not the same as the control parameter that is used by the claimed invention, which measures a voltage required to induce a current between a patterned layer of polysilicon and a substrate.

To further emphasize the differences between the Chang et al. invention and the claimed invention, the principles on which the claimed invention is based are highlighted at this time.

The claimed invention specifically concentrates on a layer of interpoly insulation and the thereto-adjacent layers of poly 1 and poly 2. In this layer of insulation, typically containing interpoly insulating material, a FN tunneling effect takes place, **which is specifically stimulated** during a FN tunneling stress phase **of the invention**.

The FN tunneling effect is typical of a thin layer of oxide that is placed under stress by an electromagnetic field that is introduced between essentially parallel surfaces of the thin layer of oxide. Under certain conditions of distance between adjacent layers of poly 1 and poly 2 and with a voltage being present across this distance, tunneling will occur in the layer of inter-poly insulation.

Fowler-Nordheim or FN tunneling occurs in layers of oxide across which an electromagnetic field in excess of 10 mV/cm occurs. In view of the extremely small thickness of a typical interpoly layer a voltage of 10 volts or more on for instance a control gate of the EPROM device will result in FN tunneling in the adjacent interpoly layer.

Otherwise stated, a charge on the poly 2 of a control gate of an EPROM device, that is created by the electron charging effect that occurs during the creation of a semiconductor device, of 10 volts or more initiates FN tunneling through the layer of interpoly insulation that is adjacent to the poly 2.

It is not uncommon the encounter such voltages of 10 volts or more, specifically during the plasma etch that is required to create openings to the source/drain regions of the gate electrode. Excessive FN tunneling is undesirable since it leads to the occurrence of positively charged ions traps in the inter-poly layer which ultimately may lead to breakdown of this layer, resulting in concerns of device reliability.

The degree to which FN funneling takes place in interface layer is in direct relation with the voltage that has been accumulated on the layer of poly 2. During FN stress test, the FN tunneling can be further stimulated. For voltages that have been accumulated on a layer of poly 2 that are relatively low, a significant amount of stimulation is required in order to initiate the FN tunneling phenomenon. The degree of stimulation that is required **before the stimulation of the stress test**

results in FN tunneling is therefore indicative of the amount of charge that has been accumulated in the layer of poly 2.

Yang provides a substrate and comments, in relation to the substrate, that a p-type or n-type conductivity dopant may be provided in the substrate. This aspect of controlling conductivity, by type and degree, of a layer of semiconductor material is well known in the art. The claimed invention has specified that the preferred implementation of the invention is to provide a substrate having a layer of n-type conductivity created in the substrate since it has been found that the method of the claimed invention can be most beneficially used with this substrate conductivity.

A number of other aspects of the claimed invention are, taken alone and not further connected to the claimed invention, well known in the art, such as the creation of a layer of gate oxide, the deposition and patterning of a layer of polysilicon and the like. These aspects taken individually have little value and only turn into a useful method or process if and when these individual aspects are combined into a new and innovative manner.

That Chang et al. invention of providing a pattern of LOCOS interspersed with exposed surface regions of the substrate suggests little or no further connection between the claimed invention and the Chang et al. invention. The creation of LOCOS regions is in many applications required to provide electrical isolation between adjacent active surface areas of a substrate. This latter is required so that a method or a process can be understood as to which surface area of the substrate the method or process is applied ("bounded" by the regions of LOCOS).

Examiner indicates that Chang does not provide for etching the exposed surface regions of the substrate, the reason for this is that Chang et al. provides for a completely different method and structure when compared with the method and structure that have been provided by the claimed invention. The claimed invention etches the substrate, using the layers of LOCOS as a hardmask, in order to provide the structure that is shown in the cross section of Fig. 10 of the claimed invention.

Chang et al. provides for a number of the instances that are kindly cited by Examiner, such as depositing a layer of polysilicon, of patterning the polysilicon. These steps in and of themselves however do not lead to the method and structure

that is provided by the claimed invention, which can again be confirmed by the reasoning that has been offered above and by comparing Figs. 1 and 2C of the Chang et al. invention with Fig. 10 of the claimed invention.

Fig. 1 of Chang et al. is a structure created over a monitoring wafer, at the time of the use of this monitoring wafer, the structure is altered from the structure shown in cross section in Fig. 1 to the structure shown in the cross section of Fig. 2C, with intervening processing steps of Figs. 2A-2C. The conversion, from Fig. 2C to Fig. 4 of the Chang et al. invention, is accomplished by applying a process that is being evaluated. The measurements that are performed on layer 14 in the cross section of Fig. 4, Chang et al. is indicative of the process that is being evaluated.

Chang et al. does not, contrary to Examiner's assertions, provide at least one contact point over the surface of the substrate.

The semiconductor processing tool that is provided by Chang et al. is provided to evaluate damage related to plasma etching

and is not used, contrary to Examiner's assertions, to evaluate electron charge effect of a process that is being performed by the tool.

Chang et al. does not, contrary to Examiner's assertions, cite in col. 6, lines 35-53, that a substrate comprises a electron charge monitoring device inside the processing tool. In the Chang et al. text cited, col. 6, lines 35-53, Chang et al. describes etching a layer of silicon oxide.

Chang et al. does not, contrary to Examiner's assertions, cite in col. 6, lines 35-53, exposing the surface of the electron charge monitoring device to established processing conditions. In the Chang et al. text cited, col. 6, lines 35-53, Chang et al. describes etching a layer of silicon oxide. Chang et al.'s approach is to use a structure, shown in the cross section of Fig. 1, modify or prepare this structure to the structure that is shown in the cross section of Fig. 2C, and expose this latter structure to a process or etch recipe that is being evaluated. The damage that is incurred by layer 14 of gate oxide is indicative of the latter process or etch recipe and is evaluated by measuring charge-to-breakdown and the breakdown field of the processed layer of gate oxide.

Chang et al. does not, contrary to Examiner's assertions, cite in col. 6, lines 54-58, terminating processing conditions. In the text cited, col. 6, lines 54-58, Chang et al. highlights one of the key aspects of the Chang et al. invention, that is the critical first exposure of the patterned layer of polysilicon during and after the etching of the spacer material, layer 22 of silicon oxide shown in the cross section of Fig. 2C of Chang et al.

Chang et al. does not, contrary to Examiner's assertions. measure a voltage required to induce a current between a layer of polysilicon and the surface of the substrate. Chang et al. depends on measuring the charge-to-breakdown and the breakdown field of an affected and potentially damaged layer of gate oxide.

With regard to claim 13, Chang et al. does not, contrary to Examiner's assertions, provide a method for the creation of an electron charge effect.

The Chang et al. invention and the Yang invention address two different aspects of creating semiconductor devices. It is

hardly a coincidence that it would be difficult to avoid any and all commonality between these two inventions. For instance both inventions use a semiconductor substrate and both apply conditions, such as temperature, photoresist and the like, for the processing of semiconductor materials and the creation of features and the like therein.

The commonality of one or more of these aspects cannot reasonably be cited as a reason as to why these two inventions would be the same or why one or more of these aspects can be copied from one invention and when applied by the second invention to result in the claimed invention.

There is in this respect no reason or motivation as to why a conductivity type that is used by Yang should be applied to the Chang et al. invention, since the Chang et al. invention at no time depends on or alludes to a conductivity type of any of the layers that are provided by Chang et al.

To further highlight the differences between Chang et al. and the claimed invention, amended claim 13, which specifies a method of creating an electron charge effect monitoring device, is quoted following, underlining in this quote the aspects of

the claimed invention that are not provided by Chang et al., as follows:

- providing a substrate, a layer of n-type conductivity having been created in the substrate
- creating a pattern of Local Oxidation of Silicon (LOCOS) regions in the substrate, the pattern of LOCOS being interspersed with exposed regions of the substrate
- etching the exposed regions of the substrate using the pattern of LOCOS regions as a hard mask, creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate
- creating a layer of interlayer oxide over the pattern of LOCOS regions and the inside surfaces of the trenches created in the substrate
- depositing a layer of polysilicon over the layer of interlayer oxide
- patterning the layer of polysilicon, the patterned layer of polysilicon comprising at least one contact point over the substrate, and
- measuring a voltage required to induce a current between the contact point of the patterned layer of polysilicon and the substrate after the substrate has been exposed to

semiconductor processing tool under known conditions of processing by the semiconductor processing tool.

From the above underlined aspects of the claimed invention, the above cited conclusions can be repeated as being equally applicable to amended claim 13 of the claimed invention, that is:

- the Chang invention provides a destructive test whereby a monitoring wafer is etched in order to evaluate a new etch recipe; the claimed invention provides a method whereby a monitoring wafer can be used without permanently affecting or damaging the monitoring wafer
- the monitor wafer of the claimed invention, after the procedure of the invention of monitoring a processing environment has been completed, can be restored to its original condition by applying an anneal to the monitor wafer; this anneal releases the trapped electron charge so that the monitor wafer can after this be re-used
- the method of the claimed invention monitors electron charging during the creation of a semiconductor device

- the method of the claimed invention makes use of electron trapping that occurs as a result of FN tunneling in a layer of interlayer oxide of an EPROM device
- the electron trapping is monitored by the claimed invention under conditions of processing. After the electron trapping has occurred, the rate of charge trapped in interlayer oxide is measured during Wafer Acceptance Testing (WAT)
- the structure that is provided by Chang et al. is significantly different from the structure that is provided by the claimed invention, as is clear when Figs. 2C and 4 provided by Chang et al. are compared with Fig. 10 of the claimed invention, and
- the parameters that are used by Chang et al. to monitor gate oxide damage, that is charge-to-breakdown and the breakdown field, are not the same as the control parameter that is used by the claimed invention, which measures a voltage required to induce a current between a patterned layer of polysilicon and a substrate.

Ahn provides a method for the creation of a high-voltage transistor and uses, as part of this invention, a step of etching a silicon substrate to a depth that is deeper than that of the field oxide film.

From the latter statement it is clear that Ahn does not provide for, as quoted in abbreviated form from amended claim 13, the essential steps of the claimed invention of creating a pattern of Local Oxidation of Silicon (LOCOS) regions in the substrate, the pattern of LOCOS being interspersed with exposed regions of the substrate, of etching the exposed regions of the substrate using the pattern of LOCOS regions as a hard mask, of thereby creating a pattern of elevated LOCOS regions, creating trenches having inside surfaces in the substrate, of creating a layer of interlayer oxide over the pattern of LOCOS regions and the inside surfaces of the trenches created in the substrate, of depositing a layer of polysilicon over the layer of interlayer oxide, of patterning the layer of polysilicon, the patterned layer of polysilicon comprising at least one contact point over the substrate, and of **measuring a voltage required to induce a current**.

The claimed invention does not address the prevention of junction breakdown, as cited by Examiner, nor does the claimed invention use junction breakdown in any manner to monitor electron charge effect occurring during semiconductor processing.

By contrast, the claimed invention makes use of electron trapping that occurs as a result of FN tunneling in a layer of interlayer oxide. The electron trapping is monitored under conditions of processing by measuring a voltage required to induce a current a said substrate.

With regard to claims 2 and 14, Chang et al. may well provide for the creating of a first pattern of LOCOS and a number of other aspects as kindly cited by Examiner, but with this Chang et al. does not provide for the method and the structure of the claimed invention, as has been highlighted in detail above and which is enclosed at this time by reference as being equally applicable to claims 2 and 14.

Claims 2 and 14 provide necessary detail for the creation of one of the aspects of the claimed invention, that is the

creation of a pattern of LOCOS regions in the substrate. These claims are dependent claims to claim 1 and 13 respectively, without the detail that is provided in claims 2 and 14 the invention would not be completely specified and might therefore be open to ambiguous interpretation or the invention might not be implementable by one skilled in the art.

With regards to claims 3 and 15, 4 and 16, 5 and 17 and claim 12, these claims are dependent claims which provide required detail in support of the independent claims. Without this supporting detail that is specified in claims 3 and 15, 4 and 16, 5 and 17 and claim 12, the invention would not be unambiguously specified or preferred conditions of implementation would be left open to arbitrary interpretation. For these and other reasons, these claims are provided, allowing one skilled in the art to implement the claimed invention.

While applicant acknowledges the teachings of over Chang et al. and Yang and Ahn as cited by the Examiner, and although applicant does not necessarily agree that the Examiner's arguments show sufficient and proper basis for suggestion or motivation to modify or combine Chang et al. and Yang and Ahn, applicant nonetheless also asserts that there is absent within

the portions of Chang et al. and Yang and Ahn or any combination thereof, as cited by the Examiner, an express or inherent teaching of each and every limitation within applicant's invention as taught and claimed within amended claims 1-5 and 12-17.

None of the applied or known references address the invention as shown in the amended claims, which concentrate on a layer of interpoly insulation and the FN tunneling effect that takes place therein, the tunneling effect being specifically stimulated during the FN tunneling stress phase of the invention, a charge on a layer of poly which is created by the electron charging effect that occurs during the creation of a semiconductor device thereby being evaluated, the degree to which FN funneling takes place in a layer of inter-poly insulation being in direct relation with the voltage that has been accumulated on the layer of poly, with the degree of stimulation that is required before FN tunneling occurs being indicative of the amount of charge that has accumulated in the layer of poly.

The invention is believed to be patentable over the prior art cited, as it is respectfully suggested that the combination

of these various references cannot be made without reference to Applicant's own invention. None of the applied references address the problem of measuring charge accumulation during semiconductor processing.

Applicant has claimed the process in detail. The processes of Figs. 4-10 and 11 are both believed to be novel and patentable over these various references, because there is not sufficient basis for concluding that the combination of claimed elements would have been obvious to one skilled in the art.

That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination. We therefore request Examiner Paul E. Brock II to reconsider the rejection in view of these arguments and the amendments to the Claims.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claims 1-5 and 12-17 under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent 6,143,579) in view of Yang (U.S. Patent 5,913,102) and Ahn (U.S. Patent 5,563,080), be withdrawn.

Claim rejections - 35 U.S.C. § 103(a)

Reconsideration of the rejection of claim 23 under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent 6,143,579) in view of Yang (U.S. Patent 5,913,102) and Ahn (U.S. Patent 5,563,080) as applied to claim 13 above and further in view of Felch et al. (U.S. Patent 4,807,994) is respectfully requested based on the following.

The relative merits of Chang et al., Yang and Ahn with respect to the claimed invention have been argued above and are enclosed at this time by reference at being equally applicable to claim 23.

Claim 23 does not specify the maintaining of a stockpile of wafers, as kindly cited by Examiner as being provided by Chang et al. Claim 23 by contrast specifies that the (read: one) electron charge effect monitoring device can be recycled by applying an additional step of thermally annealing said substrate, thereby thermally annealing the electron charge monitoring device having been created in and on the substrate.

The last paragraph on page 25 of the specification of the claimed invention states that: "The monitor wafer, after the above highlighted procedure of monitoring a processing environment has been completed, can be restored to its original condition by applying an anneal at a temperature in excess of 500 degrees C. to the monitor wafer. This anneal releases the trapped electron charge. The monitor wafer can after this be re-used."

Felch indicates, col. 6 lines 15-36, as kindly cited by Examiner, that a transmission spectrum of an implanted silicon-on-sapphire wafer can be returned to that of an un-implanted wafer by a process of anneal.

The claimed invention does not provide for an implanted silicon-on-sapphire wafer nor does the claimed invention make use of a transmission spectrum of such a wafer. The claimed invention uses trapped electron charge in a monitor wafer of special design, a design that is provided by the claimed invention, to monitor electron charge which occurs during semiconductor processing.

Felch in this respect similarly restores "something" (a wafer) to a pre-condition (of an un-implanted wafer), whereby however neither the "something" nor the applied condition (an implanted silicon-on-sapphire wafer) nor the observed phenomenon (a transmission spectrum) of Felch have any commonality with any of aspects of the claimed invention.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejection of claim 23 under 35 U.S.C. 103(a), be withdrawn.

The prior art made of record and not relied upon that is considered pertinent to Applicant's disclosure, that is Jeng et al. (U.S. Patent 6,077,740), Tabara (U.S. Patent 5,940,682), Nelson et al. (U.S. Patent 6,265,729 B1), Takeda (JP 63153863 A) and Takenaka (JP 07202018 A) have been examined and have been found to be of general interest to the invention.

Other Considerations

No new independent or dependent claims have been written as a result of this office action, no new charges are therefore incurred due to this office action.

It is requested that, should Examiner not find the claims to be allowable, to call the undersigned Attorney at the Examiner's convenience at 845-452-5863 in order to overcome any problems preventing allowance of the claims.

Respectfully submitted,

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